Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-16. (Canceled)

17. (Currently Amended) A memory array, comprising:

a plurality of stacked cells, each cell including:

a MOS transistor formed in an active region of a substrate of semiconductor material, the MOS transistor having first and second conduction regions and a control electrode;

a capacitor formed directly above ~~said active region, each of said MOS transistors having a first and a second conductive region and a control electrode and each of said capacitors~~ the first conduction region of the MOS transistor of the cell and having ~~a~~ first and ~~a~~ second ~~plate~~ plates separated by a dielectric material region; and

an electrical connector contacting a bottom of said first plate of the capacitor of the cell and connecting said first conductive region of ~~each of said MOS transistors being connected to~~ the MOS transistor of the cell to said first plate of ~~a respective capacitor~~ the capacitor of the cell;

a plurality of bit lines connected to said second conductive regions of said MOS transistors of respective cells of the plurality of stacked cells;

a plurality of word lines connected to said control electrodes of respective said MOS transistors of the plurality of stacked cells;

a plurality of plate lines connected to said second plate of respective said capacitors, said plate lines running perpendicular to said bit lines and parallel to said word lines;

wherein a pair of cells adjacent to each other in a direction parallel to said bit lines share a same dielectric material region and a same third conductive region, forming said second plates of said capacitors of said pair of cells.

18. (Original) The memory array according to claim 17, wherein said first plates of said capacitors form lower plates and said same dielectric material region runs above and between the lower plates of said two adjacent cells.

19. (Original) The memory array according to claim 18, wherein said same dielectric material region runs also on sides not facing each other of said lower plates of said two adjacent cells.

20. (Original) The memory array according to claim 17, wherein said same dielectric material region is shaped as a band running in parallel to said respective plate line.

21. (Original) The memory array according to claim 17, wherein said same third conductive region is positioned on and coextensive with said same dielectric region.

22. (Original) The memory array according to claim 21, wherein said same third conductive region has the same width as said same dielectric region, in said direction parallel to said bit lines.

23. (Original) The memory array according to claim 17, wherein said dielectric material region is made of ferroelectric material.

24. (Currently Amended) A memory array, comprising:

a substrate of semiconductor material;

a first stacked cell comprising a first transistor formed in a first active region of the substrate and a first capacitor formed above the first active region, the first capacitor having a first plate and a second plate separated by a first dielectric region;

a second stacked cell comprising a second transistor formed in a second active region of the substrate and a second capacitor formed above the second active region, the second capacitor having a first plate and a second plate separated by a second dielectric region that is

continuous with the first dielectric region, the second plate of the second capacitor being continuous with the second plate of the first capacitor; and

a third stacked cell comprising a third transistor formed in a third active region of the substrate and a third capacitor formed above the third active region, the third capacitor having a first plate and a second plate separated from each other by a third dielectric region that is continuous with the first and second dielectric regions, the second plate of the third capacitor being continuous with the second plates of the first capacitor and the second capacitor, the first and second capacitors being positioned in a first plane that is transverse to a second plane in which the second and third capacitors are positioned.

25. (Original) The memory array according to claim 24, wherein said first plates of said capacitors form lower plates and said dielectric regions are part of a dielectric layer that runs above and between the lower plates of said capacitors.

26. (Original) The memory array according to claim 25, wherein said dielectric layer runs also on sides not facing each other of said lower plates of said capacitors.

27. (Original) The memory array according to claim 24, wherein said dielectric regions are part of a dielectric layer that is shaped as a dielectric band extending in a first direction and the second plates are part of a plate line extending in the first direction in parallel to said dielectric band.

28. (Previously Presented) The memory array according to claim 27, wherein said plate line is positioned on and coextensive with said dielectric band.

29. (Original) The memory array according to claim 24, wherein said dielectric regions are made of ferroelectric material.

30. (Currently Amended) A memory array, comprising:

a substrate of semiconductor material;

a first stacked cell comprising a first transistor formed in the substrate and a first capacitor formed above the substrate, the first capacitor having a first plate and a second plate separated by a first dielectric region;

a second stacked cell comprising a second transistor formed in the substrate and a second capacitor formed above the substrate, the second capacitor having a first plate and a second plate separated by a second dielectric region that is continuous with the first dielectric region, the second plate of the second capacitor being continuous with the second plate of the first capacitor; and

a third stacked cell comprising a third transistor formed in the substrate and a third capacitor formed above the substrate, the third capacitor having a first plate and a second plate separated from each other by a third dielectric region that is continuous with the first and second dielectric regions, the second plate of the third capacitor being continuous with the second plates of the first capacitor and the second capacitor, the first and second capacitors being positioned in a first plane that is transverse to a second plane in which the second and third capacitors are positioned.

31. (Previously Presented) The memory array according to claim 30, wherein said first plates of said capacitors form lower plates and said dielectric regions are part of a dielectric layer that runs above and between the lower plates of said capacitors.

32. (Previously Presented) The memory array according to claim 31, wherein said dielectric layer runs also on sides not facing each other of said lower plates of said capacitors.

33. (Previously Presented) The memory array according to claim 30, wherein said dielectric regions are part of a dielectric layer that is shaped as a dielectric band extending in a first direction and the second plates are part of a plate line extending in the first direction in parallel to said dielectric band.

34. (Previously Presented) The memory array according to claim 33, wherein said plate line is positioned on and coextensive with said dielectric band.

35. (Previously Presented) The memory array according to claim 30, wherein said dielectric regions are made of ferroelectric material.

36. (Previously Presented) The memory array according to claim 30 wherein the first transistor is formed in a first active region of the substrate, the second transistor is formed in a second active region of the substrate, and the third transistor is formed in a third active region of the substrate.

37. (New) The memory array according to claim 17, wherein the MOS transistors of the pair of cells are positioned in separate active regions from each other, the separate active regions for the pair of cells being separated from each other by an insulating region.